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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/542,024	04/03/2000	Reinaldo A. Bergamaschi	YOR-2000-0054	4105

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FERENCE & ASSOCIATES
400 BROAD STREET
PITTSBURGH, PA 15143

EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/542,024	BERGAMASCHI ET AL.	
	Examiner	Art Unit	
	Naum B Levin	2825	AU

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,8-11,14 and 16-18* is/are rejected.

7)☒ Claim(s) *4,5,7,12,13 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 6, 8-11, 14 and 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Choukalos et al. (US Patent 6,425,109).

Choukalos discloses high level automatic core configuration including:

(1), (10), (18) A method system and computer-readable medium having computer-executable instructions for creating system of interconnecting cores in systems-on-chip, said method comprising the steps of (col.1, ll.14-36; col.7, ll.54-67; col.8, ll.30-36):

selecting/choosing at least two cores/chiplets/blocks to be interconnected, each core having at least one associated pin (col.3, ll.26-34; col.5, ll.43-51);

automatically assessing the compatibility/matching of at least one pin of at least one core with respect to at least one pin of at least one other core (col.4, ll.21-67; col.5, ll.1-25 and ll.52-67; col.6, ll.1-51); and

automatically interconnecting said cores via establishing at least one connection between at least one pair of compatible pins (col.4, ll.21-67; col.5, ll.1-25 and ll.52-67; col.6, ll.1-51);

(2) The method according to Claim 1, further comprising:

automatically assessing, subsequent to said interconnecting step, whether all pins are connected (col.6, ll.6-17);

if at least two pins are not connected, thereafter applying a protocol/algorithm/loop to establish at least one additional connection between at least one additional pair of compatible pins (col.6, ll.6-17);

(3), (6), (11), (14) The method further comprising, prior to said selecting step, classifying said cores and said pins in terms of predetermined properties (col.3, ll.55-67; col.4, ll.51-67; col.5, ll.1-25);

(8), (16) The method according to further comprising:

subsequent to said interconnecting step, automatically verifying whether the pins in at least one interconnected pair of pins have matching pin properties (col.6, ll.6-51);

(9), (17) The method according to further comprising:

prior to said verifying step, establishing a list of pin properties for which a match between the pins in at least one pair of pins is required (col.4, ll.51-67; col.5, ll.1-25);

said verifying step comprising the step of referring to said list of pin properties to determine whether the pins in at least one interconnected pair of pins have matching pin properties (col.5, ll.42-51; col.7, ll.18-27).

Allowable Subject Matter

3. Claims 4-5, 7, 12-13 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is an examiner's statement of reasons for allowance:

The prior art of record fails to teach or suggest or render obvious:

A method system and computer-readable medium having computer-executable instructions for creating system of interconnecting cores in systems-on-chip, said method comprising the steps of:

selecting/choosing at least two cores/chiplets/blocks to be interconnected, each core having at least one associated pin;

automatically assessing the compatibility/matching of at least one pin of at least one core with respect to at least one pin of at least one other core;

automatically interconnecting said cores via establishing at least one connection between at least one pair of compatible pins;

prior to said selecting step, encoding said properties as binary decision diagram variables, wherein said assessing step comprises:

performing Boolean operations on said binary decision diagram variables to compare and match properties;

performing a compatibility check to determine whether the pins of a given pair of pins are compatible with respect to at least one given property;

performing a matching check to determine whether the pins of a given pair of pins exhibit equivalent values associated with at least one given property.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bryant et al. (US Patent 4,638,442) teaches computer aided design method and apparatus which automatically generate pin-to-pin interconnection lists between respective discrete electrical component circuits. A processing unit process the entered circuit description and selected component descriptions from storage to produce an interconnection list in the form of an individual component pin to individual component pin connection.

Nishiyama et al. (US Patent 5,519,630) recites LSI automated design system in which entered pieces of external specification information are compared with one another to obtain pairs of wiring candidates of a circuit which connects, to one another, the circuit elements of the circuit to be designed. Based on the pairs of wiring candidates, there is generated wiring information which satisfies each wiring condition. Based on the pieces of wiring information thus generated, there are automatically generated circuit data of the circuit to be designed.

Morgan (US Patent 6,083,271) describes methods and apparatus for use with electronic circuit design tools to define and test multiple power and ground domains within an electronic circuit design. Power and ground signals are associated with these defined groups of devices. Lastly, this information is stored within a power and ground specification integrated with the information within the design database to allow the CAD/CAE tools to test the multiple power and ground domains within the IC or circuit board design.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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VUTHE SIEK
PRIMARY EXAMINER